What Can Intelligent SSDs Do for Machine Learning?



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| Objective | | | | Extended NVMe Stack for Machine Learning | | | |
|----------------------------|---|--|---|--|--|--------------------------|--|
| CPU | Step N-1 Storage Preprocess Transfer | Step N Storage Preprocess Transfe | Increase in accelerator performance for Machine Learning (ML) applications means | mlssd_read(HostMem, size) | This API shuffles data pages and stores it in the 'HostMem' buffer for the 'size'. We can avoid redundant data copies by utilizing NVMe's PRP list data structure and extents in Ext4 file system. | | |
| Accelerator | Model Training | Model Training | training. Usually, data input consists of retrieving data from storage to the CPU, | mlssd_get_sector(fd) | This API produces sector lists of the file('fd') based on the logical block address(LBA) and the number of blocks within the extents. | | |
| | Input Bound Training Step N-1 Step N | | preprocess operations such as shuffle, and finally transferring data to the ML accelerator. Resulting in: | ML-SSD API Device Host memory Device Host memory | | | |
| CPU Accelerator | Storage Preprocess Transfer St Model Training | torage Preprocess Transfer Model Training | Underutilizing Accelerators Longer Training Time | PRP1 reg PRP2 reg prp_list[0] | Data Page #1 Data Page #2 | PRP1 reg PRP2 reg | Data Page #1 <pre>prp_list[0]</pre> Data Page #2 |
| Accelerator Bound Training | | This project investigates intelligent storage devices for addressing the input/shuffling | prp_list[1] | Data Page #3 | | prp_list[1] Data Page #3 | |

preprocess overhead by proposing ML-SSD.

celera

CPU

MLSSD



MLSSD in a heterogeneous computer system

ML-SSD: The System Architecture and Design

The core MLSSD layer resides inside the storage device to change data resolutions presented to applications. MLSSD interacts with existing system I/O interfaces to sup-port the extended interface for resolution adjustments. MLSSD also works together with the SSD management layer to locate the desired data. The host system needs an extended kernel driver, and API functions, for the applications to send requests and exchange data. MLSSD implements the data shuffling feature in the kernel driver and API layer.

Core MLSSD Layer

The current MLSSD framework supports the following 3 categories of operators working on various data types to adjust the resolution to achieve the best performance.

Read sequence: #1, #2, #3, #4 ...

prp_list[2]

Read sequence: #2, #3, #4, #1 ...

prp_list[2]

The shuffle mechanism 1: Using PRP list

Shuffle

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Data Packing The data packing operator trims the dataset size by using fewer bytes to express each item and condenses the layout in memory. This operator is suitable for datasets using only a small range within the number space of the original data type, or the applications which can tolerate some inaccuracy in the input data, e.g. FP64 to FP32.



Sample The sample operator chooses a subset of items from raw data and sends the selected items to the host computer. This operators can perform uniform data selection, random data selection, or only report the most representative data. The sample operator helps filter repetitive or similar inputs. If the compute kernel is elastic to the number of records within the dataset, the sample operator can achieve the same effect as loop perforation without any code modification.



0x0000<mark>1234</mark>

0x0000<mark>5678</mark>

Data Packing

0x<mark>12345678</mark>

Data Packing Operator

Reduction The reduction operator applies a function

(e.g., average) to groups of input values, usually

neighboring data items in the raw data, and

generate a single output for each group. Thus,

MLSSD only sends out the resulting values of each

group to reduce the amount of data going through the

MLSSD hides the latency of altering input datasets with accessing flash chips while taking advantages of richer internal parallelism, MLSSD accelerates the process of reading data inputs by 1.55x.



Shuffle mechanism1: Using PRP list

Sampling Operator

Shuffle mechanisms minimize memory copies compared to convention shuffle. Using PRP list, it shows a speedup of 1.23x when the read size is 1MB.

The prototype SSD

system interconnect.



We build a MLSSD by extending a commercialized datacenter-class SSD. We extended the NVMe driver in this system to support additional MLSSD NVMe commands. This SSD runs our modified firmware programs which is also compatible with standard NVMe. Throughout our tests, the baseline SSD achieves 3.2 GB/s bandwidth to the host system.



Shuffle mechanism2: Using Extents

The result shows that by partition requests into 8 MB chunks, MLSSD can speedup reads by 1.32x, in addition to the performance gain from moving data adjustments into the SSD.

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